

IBM Docket No. RPS920010127US1 - PATENT

2133
#3/4-2002
V-Jerry

In the United States Patent and Trademark Office

Date: April 8, 2002

In re Application of: R. T. Bailis, et al.

Serial Number: 10/016,449

Filed: Dec. 10, 2001

For: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC

Group Art Unit: 2133

RECEIVED

APR 18 2002

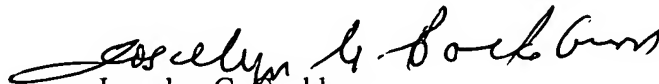
Technology Center 2100

Assistant Commissioner of Patents
Washington, DC 20231

TRANSMITTAL OF FORMAL DRAWINGS

Attached please find formal drawings (3 sheets) for the above-identified application.

Respectfully submitted,


Joscelyn G. Cockburn

Attorney of Record, Reg. No: 27,069

IBM Corporation 9CCA/B002
P.O. Box 12195
Research Triangle Park, NC 27709
Telephone: 919-543-9036
Fax: 919-254-2649

Certificate of Mailing (37 CFR 1.8a)

I hereby certify this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks; Washington, DC 20231

Date: April 11, 2002



Karen Orzechowski